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Rev. 01R3.30_20230817

40G QSFP+ PSM4 IR Transceiver
Hot Pluggable, MPO / MTP, 1310nm DFB, SMF 2KM, DDM

Part Number: FQFP-I9-S13-02D

Overview

FQFP-I9-S13-02D is a Four-Channel Parallel SM Fibers QSFP+ transceiver for 40GbE and InfiniBand DDR, QDR, SDR application especially in Data Center & Storage networks. The QSFP full-duplex optical module with MPO-12 receptacle offers 4 independent transmitter and receiver channels each capable of 10.3Gbps operation for an aggregate data rate of 41.2Gbps up to SMF 2km optical links.

Applications

- 40Gb Ethernet
- OTN OTU3 @43.01G, OTU3e2 @44.58G
- Breakout to 4 x 10GBASE-LR Ethernet
- InfiniBand DDR, QDR, SDR interconnects
- Data Center & Storage
- Datacom / Telecom Switch & Router

Features

- Compatible with IEEE802.3ba 40GBASE-LR4
- Compliant to SFF-8436 QSFP+ MSA
- Supports QDR, DDR & SDR InfiniBand
- 4 independent full-duplex channels
- Up to 11.2Gbps data rate per channel
- Hot Pluggable
- 1310nm DFB array transmitter
- MPO-12 receptacle connector
- 2-wire interface for management and diagnostic monitor compliant with SFF-8436, SFF-8636
- Single 3.3V power supply
- Link distance 2km over SM fiber
- Power consumption < 2.5W
- RoHS compliant

Laser Safety

- This is a Class 1 Laser Product complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.
- Caution: Use of control or adjustments or performance of procedure other than those specified herein may result in hazardous radiation exposure.

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Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Storage Temperature	T_{ST}	-40	+85	°C
Storage Relative Humidity	RH	5	85	%
Supply Voltage	V_{CC3}	-0.5	+3.6	V

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Unit
Case Operating Temperature	T_{OP}	0	-	+70	°C
Supply Voltage	V_{CC}	+3.13	+3.3	+3.47	V
Data Rate, per Lane	DR		10.3125		Gb/s
Data Rate Accuracy	ΔDR	-100		+100	ppm
Bit Error Rate	BER			10^{-12}	
Supply Current	I_{CC}			700	mA
Power Consumption	P		1.7	2.5	W
Transceiver Power-on Initialization Time				2000	ms

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Transmitter Electro-optical Characteristics

V_{CC} = 3.13V to 3.47V, T_{OP} = 0 °C to 70 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Data Rate, per Lane	DR		10.3125		Gb/s	
Average Launch Power, per Lane	P_{AVG}	-5.5	-0.5	+2.3	dBm	
Optical Modulation Amplitude (OMA), per Lane	P_{OMA}	-4.5	-0.5	+2.5	dBm	1
Launch Power in OMA minus Transmitter and Dispersion Penalty, per Lane	OMA-TDP	-9.7			dB	1
Difference in Launch Power between any two Lanes	$P_{TX-DIFF}$			5.0	dB	
Optical Wavelength	λc	1270	1310	1350	nm	1
Spectral Width (-20dB)	Δλ			1	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Optical Extinction Ratio	ER	3.5			dB	
Optical Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Average Launch Power OFF, per Lane	P_{OFF}			-30	dBm	
Relative Intensity Noise	RIN			-128	dB/Hz	
Optical Return Loss Tolerance	ORLT			12	dB	
Transmitter Reflectance	P_T			-12	dB	
Input Differential Impedance	Z_{IN}	90	100	110	Ω	
Differential Data Input Voltage	V_{IN-PP}	300		1100	mVpp	
Control I/O Voltage, High	V_{IH}	2.0		Vcc	V	
Control I/O Voltage, Low	V_{IL}	GND		0.8	V	

Note1: Transmitter wavelength and launch power need to meet the OMA minus TDP specs to guarantee link performance.

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Receiver Electro-optical Characteristics

V_{CC} = 3.13V to 3.47V, T_{OP} = 0 °C to 70 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Data Rate, per Lane	DR		10.3125		Gb/s	
Damage Threshold, per Lane	D_{TH}	+3.0			dBm	1
Average Receive Power, per Lane	P_{RX-AVG}	-11.5		+2.3	dBm	
Receiver Power (OMA), per Lane				+2.5	dBm	
Receive Sensitivity (OMA), per Lane	P_{RX-OMA}			-11.5	dBm	2
Difference in Receive Power between any two Lanes (OMA)	$P_{RX-DIFF}$			5.0	dB	
Center Wavelength	λc	1270	1310	1350	nm	
Optical Return Loss	ORL			-12	dB	
LOS De-Assert	LOS_D			-15	dBm	
LOS Assert	LOS_A	-30			dBm	
LOS Hysteresis	LOS_{HY}	0.5			dB	
Output Differential Impedance	Z_{OUT}	90	100	110	Ω	
Differential Data Output Voltage	V_{OUT-PP}	500		800	mVpp	

Note1: The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

Note2: Measured with conformance test signal at receiver input for BER= $1x10^{-12}$.

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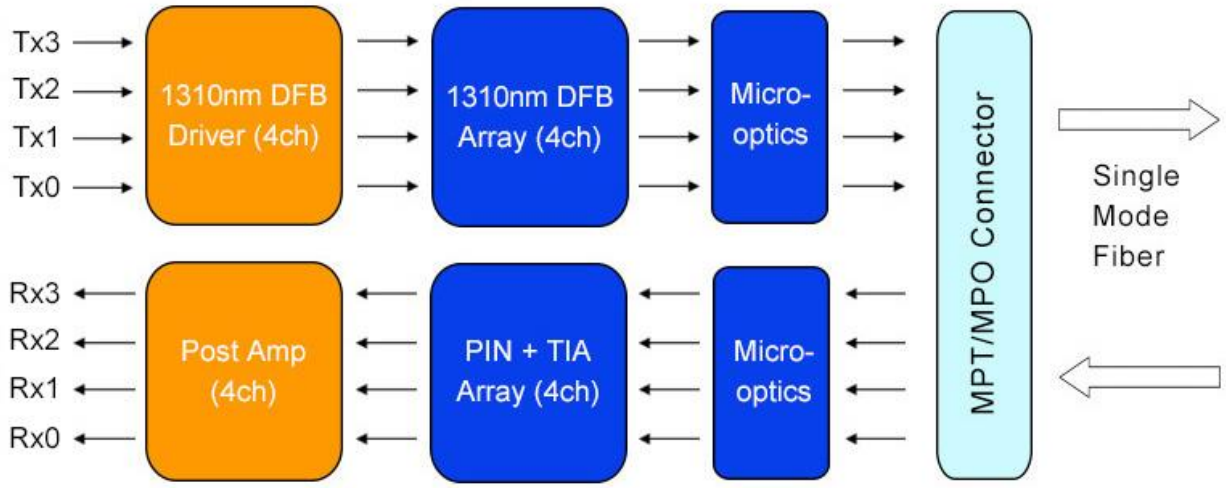
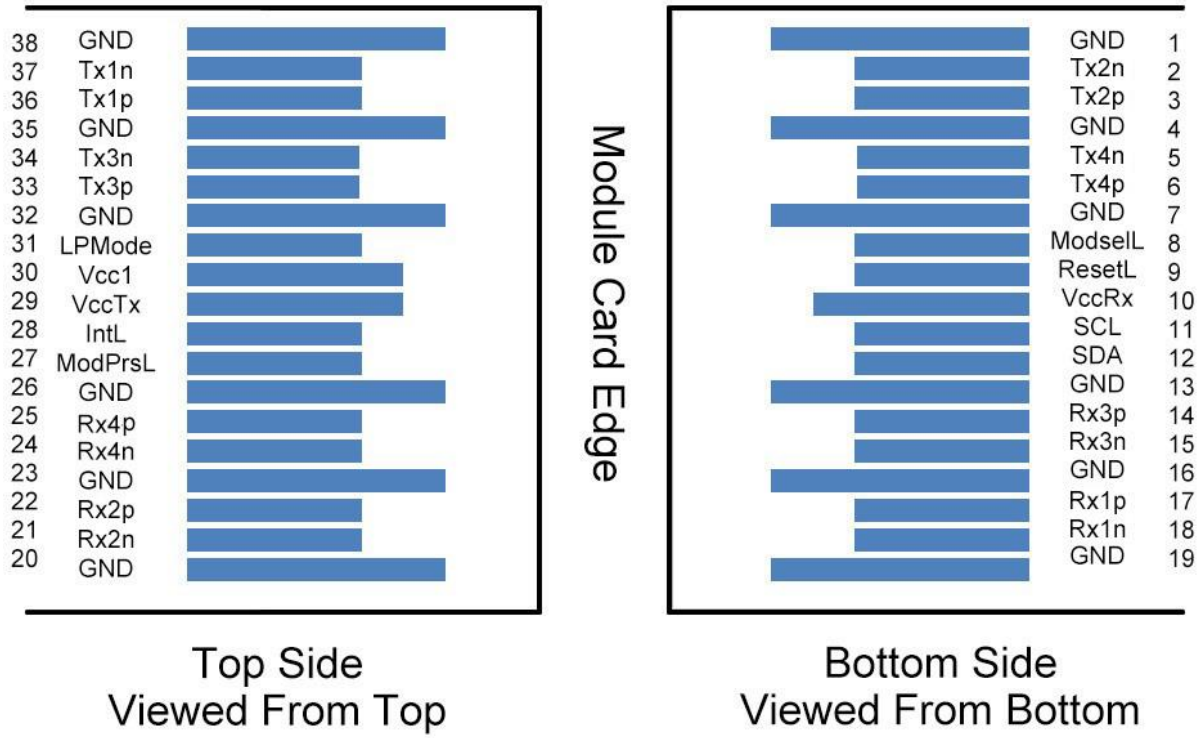
Transceiver Block Diagram



Pin Assignment



Top Side
Viewed From Top

Bottom Side
Viewed From Bottom

Pin Description

Pin	Logic	Name	Function / Description
1		GND	Module Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Module Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Module Ground
8	LVTLL-I	ModSelL	Module Select
9	LVTLL-I	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data
13		GND	Module Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Module Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Module Ground
20		GND	Module Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Module Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Module Ground
27	LVTLL-O	ModPrsL	Module Present
28	LVTLL-O	IntL	Interrupt
29		VccTx	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTLL-I	LPMode	Low Power Mode
32		GND	Module Ground

33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Module Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Module Ground

Note1: GND is the symbol for signal and supply (power) common for QSFP+ modules. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground lane.

Note2: VccRx, Vcc1 and VccTx are the receiver and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRx, Vcc1 and VccTx may be internally connected within the QSFP+ transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

Digital Diagnostic Functions

As defined by the QSFP+ MSA, Ficer's QSFP+ transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

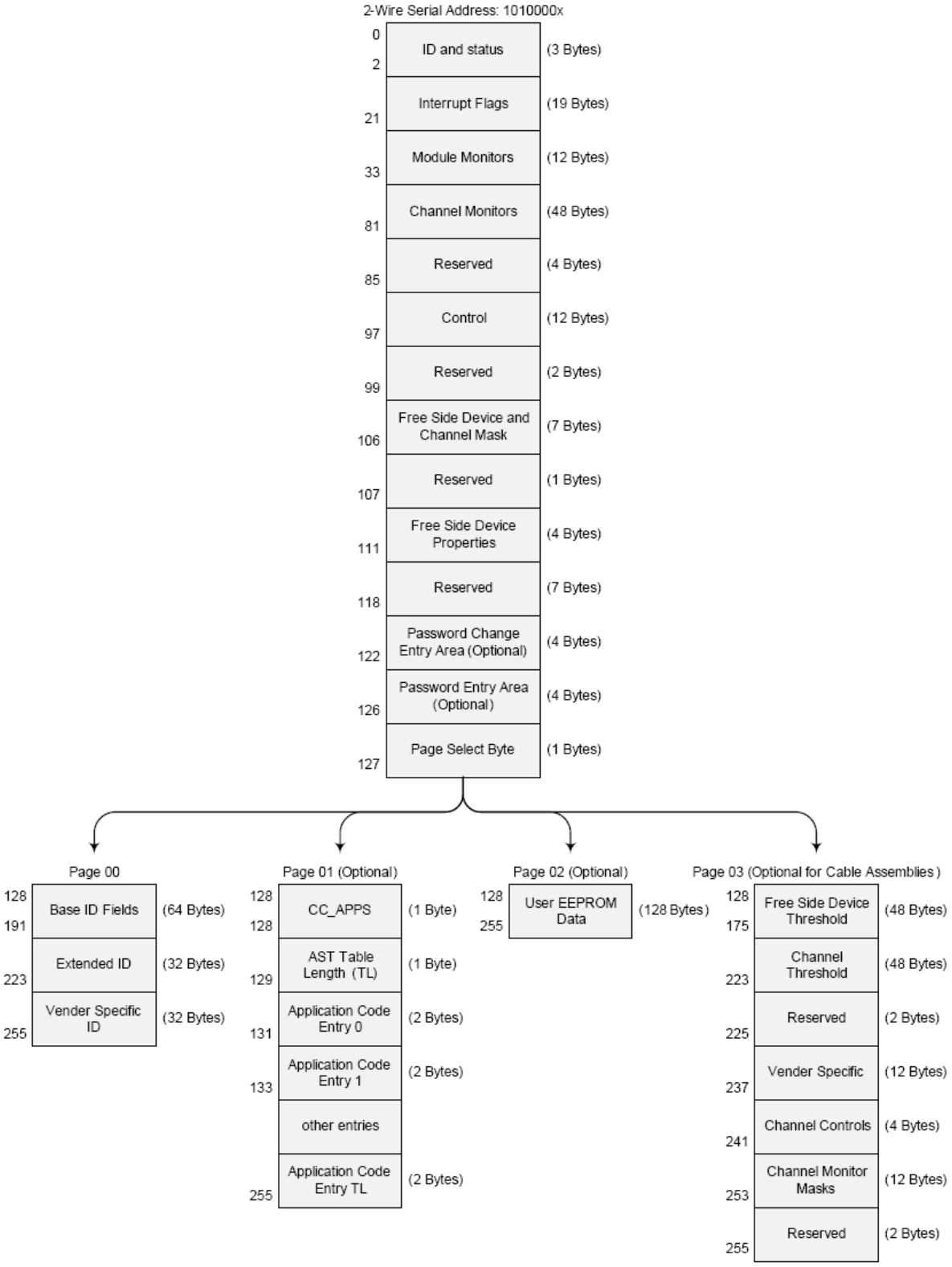
- Transceiver temperature
- Laser bias current (4-Channel)
- Transmitted optical power (4-Channel)
- Received optical power (4-Channel)
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Controller (DDC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP+ transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the QSFP+ transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information including memory map definitions, please see the QSFP+ MSA Specification.

Digital Diagnostic Memory Map


2-Wire Serial Address: 1010000x
0
2
ID and status
(3 Bytes)
21
Interrupt Flags
(19 Bytes)
33
Module Monitors
(12 Bytes)
81
Channel Monitors
(48 Bytes)
85
Reserved
(4 Bytes)
97
Control
(12 Bytes)
99
Reserved
(2 Bytes)
106
Free Side Device and Channel Mask
(7 Bytes)
107
Reserved
(1 Bytes)
111
Free Side Device Properties
(4 Bytes)
118
Reserved
(7 Bytes)
122
Password Change Entry Area (Optional)
(4 Bytes)
126
Password Entry Area (Optional)
(4 Bytes)
127
Page Select Byte
(1 Bytes)
Page 00
128
191
Base ID Fields
(64 Bytes)
223
Extended ID
(32 Bytes)
255
Vender Specific ID
(32 Bytes)
Page 01 (Optional)
128
128
CC_APPS
(1 Byte)
129
AST Table Length (TL)
(1 Byte)
131
Application Code Entry 0
(2 Bytes)
133
Application Code Entry 1
(2 Bytes)
other entries
255
Application Code Entry TL
(2 Bytes)
Page 02 (Optional)
128
255
User EEPROM Data
(128 Bytes)
Page 03 (Optional for Cable Assemblies)
128
175
Free Side Device Threshold
(48 Bytes)
223
Channel Threshold
(48 Bytes)
225
Reserved
(2 Bytes)
237
Vender Specific
(12 Bytes)
241
Channel Controls
(4 Bytes)
253
Channel Monitor Masks
(12 Bytes)
255
Reserved
(2 Bytes)

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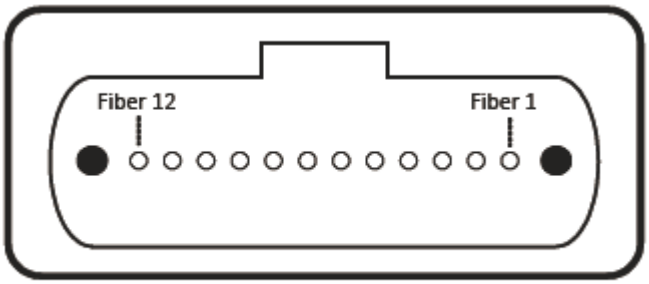
Optical Interface Lanes and Assignment



Outside view of the QSFP module MPO

Fiber #	Lane Assignment
1	Rx0
2	Rx1
3	Rx2
4	Rx3
5,6,7,8	Not used
9	Tx3
10	Tx2
11	Tx1
12	Tx0

lane assignment

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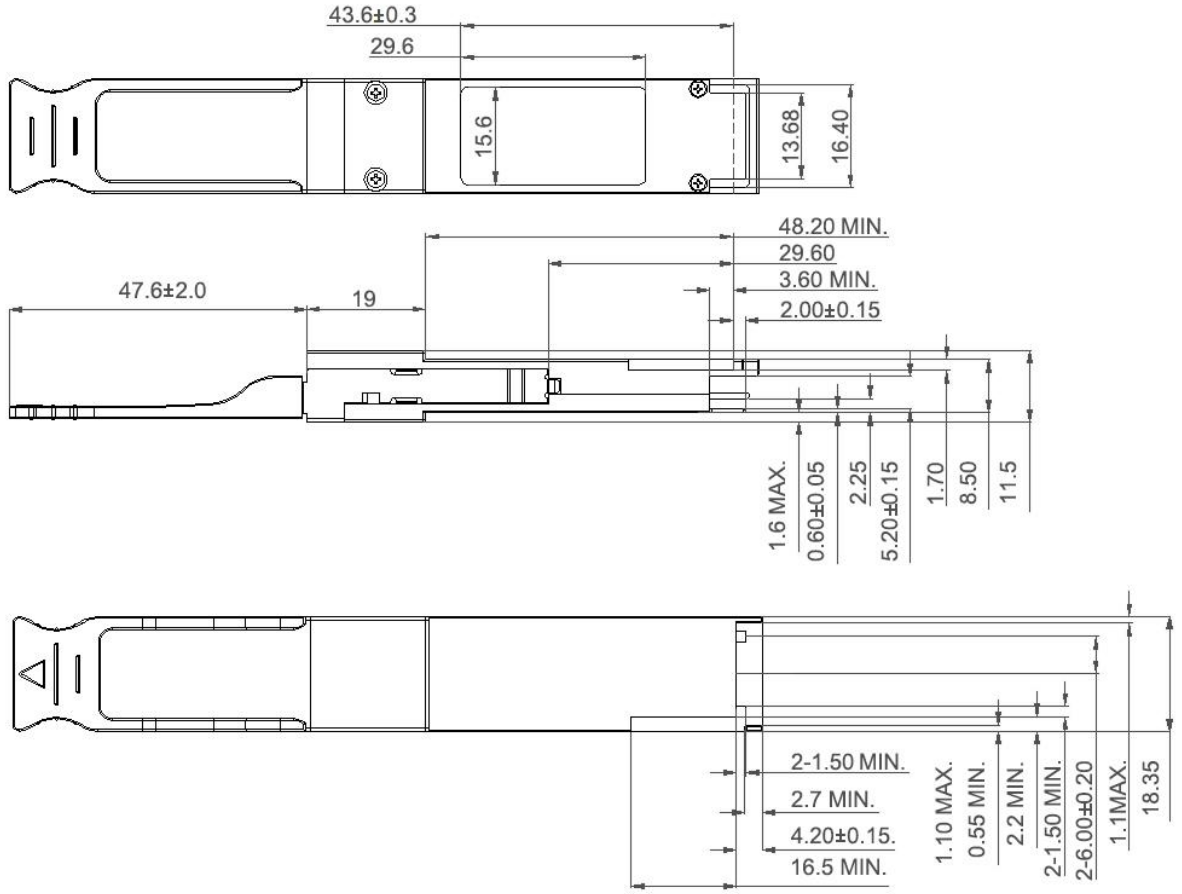
Mechanical Dimensions



(All Dimensions are ±0.20mm Unless Otherwise Specified, Unit: mm)

Ordering Information

Part No.	Tx	Rx	Link	DDM	Temp.
FQFP-I9-S13-02D	1310 nm	1310 nm	2km	Yes	0~70°C

Note1: Distances are indicative only. To calculate a more precise link budget based on specific conditions in your application, please refer to the optical characteristics.

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